IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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In re Patent Application of:

Shunpei YAMAZAKI et al.

Application No. 09/837,558

Filed: April 19, 2001

For: SEMICONDUCTOR DEVICE AND

MANUFACTURING METHOD

THEREOF

) Group Art Unit: 2814

) Examiner: Nathan W. Ha

Confirmation No. 7532

Date: May 12, 2004

CERTIFICATE OF MAILING OR TRANSMISSION [37 CFR 1.8(a)]

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Signature: Neborah Worakhedi

Name: Deborah Movahhedi

REQUEST FOR RECONSIDERATION

Mail Stop: AFTER FINAL Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

In response to the Office Action mailed February 12, 2004, please consider the remarks in connection with the above-identified application as follows.

REMARKS

The Examiner's Office Action of February 12, 2004 has been received and its contents reviewed. Applicants would like to thank the Examiner for the consideration given to the above-identified application.

Claims 31-50 are pending for consideration, of which claims 31, 33, 36, 39, 42, 45 and 48 are independent. In view of the following remarks, reconsideration of this application is now requested.

Referring now to the detailed Office Action, claims 31-50 stand rejected under 35 U.S.C. §102(e) as anticipated by previously cited Yamazaki et al. (U.S. Patent No. 6,603,453 - hereinafter Yamazaki '453). This rejection is respectfully traversed at least for the reasons provided below.

In the Office Action, the Examiner asserts that Yamazaki '453 discloses the feature wherein the active layer of the n-channel TFT is located over the first wiring line with the first insulating film interposed therebetween and the active layer of the p-channel TFT does not overlap any portion of the first wiring line. The Examiner only cites Fig. 18b of Yamazaki as providing support for the assertion in which active regions do not overlap the first metal layer.

In response to the Examiner's assertion, Applicants respectfully submit that the Examiner's assertion is insupportable for the reason that Yamazaki '453 discloses that all of the active regions are overlapped with the first wiring lines. As shown in Fig. 18b of Yamazaki '453, all three regions with slash marks under the underlying film 1703 in Fig. 18B are back gate electrode 1702. A detailed description of Fig. 18B can be found in column 30, lines 28-61, of Yamazaki '453. Applicants note that, although one of the regions is not explicitly labeled in Fig. 18b as back gate electrode, it can be understood that the region is a back gate electrode. Hence, Yamazaki '453 does not disclose that the active layer of the p-channel TFT does not overlap any portion of the first wiring line recited in claim 31, and Yamazaki '453 does not disclose the second semiconductor island not overlapping any portion of the first conductive film recited in claims 33, 36, 39, 42, 45 and 48.

Should the Examiner maintain the assertion that Fig. 18B of Yamazaki '453 discloses active regions not overlapping the first metal layer, Applicants will request the Examiner to be specific in helping Applicants to understand where in Fig. 18B that feature is shown.

In view of the amendments and arguments set forth above, Applicants respectfully request reconsideration and withdrawal of all the pending rejections.

While the present application is now believed to be in condition for allowance, should the Examiner find some issue to remain unresolved, or should any new issues arise, which could be eliminated through discussions with Applicants' representative, then the Examiner is invited to contact the undersigned by telephone in order that the further prosecution of this application can thereby by expedited.

Respectfully submitted,

Luan C. Do

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AF/28/4. 09/837,558 **Application Number** TRANSMITTAL Filing Date April 19, 2001 **FORM** (to be used for all correspondence after initial filing) First Named Inventor Shunpei YAMAZAKI et al. Group Art Unit 2814 **Examiner Name** Nathan W. Ha Attorney Docket Number 740756-2297 Total Number of Pages in This Submission ENCLOSURES (check all that apply) After Allowance Communication to Group ☐ Fee Transmittal Form ■ Assignment Papers (for an Application) Appeal Communication to Board of Fee Attached Appeals and Interferences Drawing(s) Appeal Communication to Group (Appeal Notice, Brief, Reply Brief) Request for Reconsideration/ Reply Declaration and Power of Attorney Proprietary Information Licensing-related Papers After Final Status Letter Petition Affidavits/declaration(s) Application Data Sheet Petition to Convert to a Provisional Extension of Time Request Request for Corrected Filing Receipt with Application Enclosures Power of Attorney, Revocation Express Abandonment Request A self-addressed prepaid postcard for Change of Correspondence Address acknowledging receipt Information Disclosure Statement Terminal Disclaimer Other Enclosure(s) (please identify below): Certified Copy of Priority PTO-1449 Form w/1 document Request for Refund Document(s) CD, Number of CD(s) Response to Missing Parts/ Incomplete Application Response to Missing Parts under 37 CFR 1.52 or 1.53 Remarks The Commissioner is hereby authorized to charge any additional fees required or credit any overpayments to Deposit Account No. 19-2380 for the above identified docket number. SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT Firm Luan C. Do, Reg. No. 38,434 Nixon Peabody LLP Individual name 401 9th Street, N.W. Suite 900 n, D.C. 20004-2128 Washingt Signature May 12 Date CERTIFICATE OF MAILING OR TRANSMISSION [37 CFR 1.8(a)] I hereby certify that this correspondence is being: deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop AF, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450 □ transmitted by facsimile on the date shown below to the United States Patent and Trademark Office at (703)5-12-04

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